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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,500	01/23/2002	Michael Kagan	3891-0104P	4997

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EXAMINER	
NANO, SARGON N	

ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,500	KAGAN ET AL.	
	Examiner	Art Unit	
	Sargon N. Nano	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1- 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application filed on Jan. 23, 2002. Claims 1 – 28 are pending examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Gronke U.S .Patent No. 6,888,792

As to claim 1,Gronke teaches a method for communication over a network, comprising: assigning one or more doorbell addresses on a network interface adapter for use by a host processor (see co. 2 line 56 – col. 3 line 22 and fig.1B, Gronke discloses many descriptors that include address segments);

writing a first descriptor to a system memory associated with the host processor, the first descriptor defining a first message to be sent over the network; writing a command to a first one of the doorbell addresses instructing the adapter to read and execute the first descriptor(see co. 2 line 56 – col. 3 line 22 and fig.1B, Gronke discloses descriptors that identify send/receive operation);

writing a second descriptor to a second one of the doorbell addresses, the second descriptor defining a second message to be sent over the network (see co. 2 line 56 – col. 3 line 22 and fig.1B, Gronke discloses descriptors that identify send/receive operation);

responsive to the command having been written to the first one of the doorbell addresses, reading the first descriptor from the system memory using the network interface adapter, and sending the first message from the network interface adapter over the network responsive to the first descriptor (see col. 2 line 56 – col. 3 line 32 and fig. 1 B, Gronke discloses sending from network interface to a network); and

responsive to the second descriptor having been written to the second one of the doorbell addresses, sending the second message from the network interface adapter over the network(see col. 2 line 56 – col. 3 line 32 and fig. 1 B, Gronke discloses sending from network interface to a network).

As to claim 2, Gronke teaches a method according to claim 1, wherein assigning the one or more doorbell addresses comprises allocating a priority area for writing the descriptors within an address range defined by the one or more doorbell addresses, and wherein writing the second descriptor comprises writing the second descriptor to the priority area (see col. 9 lines 42 – 58).

As to claim 3, Gronke teaches a method according to claim 2, wherein writing the second descriptor to the priority area comprises writing the second descriptor after writing the command to the first one of the doorbell addresses, and wherein sending the second message comprises, responsive to writing the second descriptor to the priority

area, sending the second message before sending the first message (see col. 9 lines 42 – 64).

As to claim 4, Gronke teaches a method according to claim 2, wherein writing the second descriptor comprises writing the second descriptor to the system memory, as well as to the priority area, and wherein sending the second message comprises, when the second descriptor is successfully written in its entirety to the priority area, executing the second descriptor written to the priority area without reading the second descriptor from the system memory(see col. 9 lines 42 – 64).

As to claim 5, Gronke teaches a method according to claim 1, wherein writing the first and second descriptors comprises indicating first and second ranges of data to be read from the system memory for inclusion in the first and second messages, respectively, and wherein sending the first and second messages comprises reading the data from the first and second ranges responsive to the first and second descriptors(see col. 9 lines 42 – 64).

As to claim 6, Gronke teaches a method according to claim 5, wherein reading the data comprises reading the data using direct memory access (DMA) by the network interface adapter to the system memory(see col. 3 lines 58 – col.4 line 13).

As to claim 7, Gronke teaches a method according to claim 1, wherein assigning the one or more doorbell addresses comprises assigning first and second doorbell addresses respectively to first and second processes running on the host processor, and wherein writing the command comprises writing the command to the first doorbell address using the first process, and writing the second descriptor comprises writing the

second descriptor to the second doorbell address using the second process (see col. 3 line 58 – col.4 line 13).

As to claim 8, Gronke teaches a method according to claim 1, wherein sending the first and second messages comprises sending one or more data packets over the network for each of the messages (see col. 5 lines 47 – 62).

As to claim 9, Gronke teaches a method according to claim 8, wherein the network comprises a switch fabric, and wherein the network interface adapter comprises a host channel adapter (HCA), and wherein writing the first and second descriptors comprises submitting work requests (WRs) for execution by the HCA. (see col. 2 line 49 – col. 3 line 22 and fig. 3).

As to claim 10, Gronke teaches a method for direct memory access (DMA), comprising: writing a first descriptor to a system memory associated with a host processor, the first descriptor defining a first operation for execution by a DMA engine(see col 3 lines 33 – 57); writing a command to a first doorbell address of the DMA engine, instructing the engine to read and execute the first descriptor(see col. 3 line 58 – col. 4 line 13); writing a second descriptor to a second doorbell address of the DMA engine, the second descriptor defining a second operation for execution by the DMA engine(see col. 3 line 58 – col. 4 line 13); responsive to the command written to the first doorbell address, reading the first descriptor from the system memory and executing the first descriptor using the DMA engine (see col.3 line 58 – col. 4 line 13); and responsive to the second descriptor having been written to the second doorbell

address, executing the second descriptor using the DMA engine (see col.3 line 58 – col. 4 line 13).

As to claim 11, Gronke teaches a method according to claim 10, wherein writing the second descriptor comprises writing the second descriptor to a priority area allocated for writing the descriptors within an address range of the doorbell addresses (see col.9 lines 42 – 58).

As to claim 12, Gronke teaches a method according to claim 11, wherein writing the second descriptor to the priority area comprises writing the second descriptor after writing the command to the first doorbell address, and wherein executing the second descriptor comprises, responsive to writing the second descriptor to the priority area, executing the second descriptor before executing the first descriptor(see col.9 lines 42 – 58).

As to claim 13, Gronke teaches a method according to claim 11, wherein writing the second descriptor comprises writing the second descriptor to the system memory, as well as to the priority area, and wherein executing the second descriptor comprises, when the second descriptor is successfully written in its entirety to the priority area, reading and executing the second descriptor written to the priority area using the DMA engine, without reading the second descriptor from the system memory(see col.9 lines 42 – 58).

As to claim 14, Gronke teaches a method according to claim 10, wherein writing the first and second descriptors comprises indicating first and second address ranges, respectively, in the system memory, and wherein executing the first and second

descriptors comprises at least one of a scatter step, comprising conveying data from a data source to at least one of the first and second address ranges, and a gather step, comprising conveying data from at least one of the first and second address ranges to a data target (see col.9 lines 42 – 58).

As to claim 15, Gronke teaches a network interface adapter, for coupling a host processor to a communication network, the adapter comprising:

a range of doorbell addresses in an address space of the host processor, the range including first and second doorbell addresses (56 – col. 3 line 22 and fig.1B);

execution circuitry, adapted to send messages over the network responsive to descriptors prepared by the host processor, the descriptors including first and second descriptors (see col. 9 line 42 – 64 fig. 3); and

a doorbell handler, which is coupled to the range of doorbell addresses so as to receive a command written by the host processor to the first doorbell address, indicating that the first descriptor has been written to a system memory associated with the host processor, the first descriptor defining a first one of the messages, and so as to receive the second descriptor written by the host processor to the second doorbell address, the second descriptor defining a second one of the messages, the doorbell handler being further coupled, responsive to the command having been written to the first doorbell address, to instruct the execution circuitry to read the first descriptor from the system memory and to execute the first descriptor so as to send the first one of the messages, and responsive to the second descriptor having been written to the second doorbell address, to pass the second descriptor to the execution circuitry and to instruct the

execution circuitry to execute the second descriptor so as to send the second one of the messages (see col. 9 lines 42 – 64 and figs. 9 and 1B).

As to claim 16, Gronke teaches an adapter according to claim 15, wherein the second doorbell address is in a priority area within the address range, allocated for writing the descriptors thereto by the host processor (see col. 9 lines 42 – 64 and fig. 9).

As to claim 17, Gronke teaches an adapter according to claim 16, wherein the execution circuitry comprises a scheduler, which is adapted to determine an order of execution of the descriptors by the execution circuitry, and wherein responsive to the second descriptor having been written to the priority area, the doorbell handler is adapted to place the second descriptor in the order for execution ahead of the first descriptor(see col. 9 lines 42 – 64 and fig. 9).

As to claim 18, Gronke teaches an adapter according to claim 16, wherein the second descriptor is written by the host processor to the system memory, as well as to the priority area, and wherein the doorbell handler is adapted, when the second descriptor is successfully written in its entirety to the priority area, to pass the second descriptor to the execution circuitry without instructing the execution circuitry to read the second descriptor from the system memory(see col. 9 lines 42 – 64 and fig. 9).

As to claim 19, Gronke teaches an adapter according to claim 15, wherein the first and second descriptors indicate first and second ranges of data to be read from the system memory for inclusion in the first and second messages, respectively, and wherein the execution circuitry is adapted to read the data from the first and second ranges responsive to the first and second descriptors(see col.9 lines 42 – 58).

As to claim 20, Gronke teaches an adapter according to claim 19, wherein the execution circuitry comprises a gather engine, which is coupled to read the data by direct memory access (DMA) to the system memory(see col.3 line 56 – col. 4 line 13).

As to claim 21, Gronke teaches an adapter according to claim 15, wherein the first and second doorbell addresses are assigned respectively to first and second processes running on the host processor, and wherein the command is written to the first doorbell address using the first process, and the second descriptor is written to the second doorbell address using the second process(see col. 2 line 56 – col. 3 line 32).

As to claim 22, Gronke teaches an adapter according to claim 15, wherein the execution circuitry is adapted to send the first and second messages by generating data packets to send over the network for each of the messages.

As to claim 23, Gronke teaches an adapter according to claim 22, wherein the network comprises a switch fabric, and wherein the network interface adapter comprises a host channel adapter (HCA), and wherein the first and second descriptors comprise work requests (WRs) submitted by the host processor for execution by the HCA.(see col. 2 line 49 – col. 3 line 22).

As to claim 24, Gronke teaches a host channel adapter, for coupling a host processor to a switch fabric, the adapter comprising:

a range of doorbell addresses in an address space of the host processor, the range including first and second doorbell addresses(56 – col. 3 line 22 and fig.1B);

execution circuitry, adapted to generate data packets for transmission over the network responsive to work requests prepared by the host processor, the work requests including first and second work requests(see col. 9 line 42 – 64 fig. 3); and

a doorbell handler, which is coupled to the range of doorbell addresses so as to receive a command written by the host processor to the first doorbell address, indicating that the first work request has been written to a system memory associated with the host processor, and so as to receive the second work request written by the host processor to the second doorbell address, the doorbell handler being further coupled, responsive to the command having been written to the first doorbell address, to pass instructions to the execution circuitry to read the first work request from the system memory and to execute a first work queue element corresponding to the first work request so as to generate the data packets called for by the first work request, and responsive to the second work request having been written to the second doorbell address, to pass a work queue element corresponding to the second work request to the execution circuitry and to instruct the execution circuitry to execute the second work queue element so as to generate the data packets called for by the second work request(see col. 9 lines 42 – 64 and figs. 9 and 1B).

As to claim 25, Gronke teaches a direct memory access (DMA) device, comprising:

a range of doorbell addresses in an address space of a host processor, the range including first and second doorbell addresses(56 – col. 3 line 22 and fig.1B);

a DMA engine, adapted to access a system memory associated with the host processor, responsive to descriptors prepared by the host processor, the descriptors including first and second descriptors defining respective first and second operations for execution by the DMA engine(see col. 3 lines 58 – col.4 line 13); and

a doorbell handler, which is coupled to the range of doorbell addresses so as to receive a command written by the host processor to the first doorbell address, indicating that the first descriptor has been written to the system memory, and so as to receive the second descriptor written by the host processor to the second doorbell address, the doorbell handler being further coupled, responsive to the command having been written to the first doorbell address, to instruct the DMA engine to execute the first operation responsive to the first descriptor in the system memory, and responsive to the second descriptor having been written to the second doorbell address, to instruct the DMA engine to execute the second operation(see col. 9 lines 42 – 64 and figs. 9 and 1B).

As to claim 26, Gronke teaches a device according to claim 25, wherein the second doorbell address is in a priority area within the address range, allocated for writing the descriptors thereto by the host processor(see col. 9 lines 42 – 64 and fig. 9).

As to claim 27, Gronke teaches a device according to claim 26, and comprising a scheduler, which is adapted to determine an order of execution of the operations by the DMA engine, and wherein responsive to the second descriptor having been written to the priority area, the doorbell handler is adapted to place the second operation in the order for execution ahead of the first operation. (see col. 9 lines 42 – 64 and fig. 9) .

As to claim 28, Gronke teaches a device according to claim 26, wherein the second descriptor is written by the host processor to the system memory, as well as to the priority area, and wherein the doorbell handler is adapted, when the second descriptor is successfully written in its entirety to the priority area, to pass the second descriptor to the DMA engine for execution without reading the second descriptor from the system memory. (see col. 9 lines 42 – 64 and fig. 9).

As to claim 29, Gronke teaches a device according to claim 25, wherein the first and second descriptors indicate first and second address ranges, respectively, in the system memory, and wherein the first and second operations executed by the DMA engine comprise at least one of a scatter operation, comprising conveying data from a data source to at least one of the first and second address ranges, and a gather operation, comprising conveying data from at least one of the first and second address ranges to a data target. (see col.9 lines 42 – 58).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sargon N. Nano whose telephone number is (571) 272-4007. The examiner can normally be reached on 8 hour.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sargon Nano
Sep. 6, 2005

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